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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 16

Application Number: 09/346,436
Filing Date: 07/01/99
Appellant(s): Theodore W. Houston

Jay M. Cantor
For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed 6/27/01.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that the claims do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct except for, in claim 1, the step (c) is used twice where (d) should have been used.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

5,087,585	Hayashi	2/11/92
Applicant's Admitted Prior Art		

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims **1**, 3, 7-9 and **18**-21, 23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by **Hayashi** (US 5,087,585).

Regarding claims 1 and 3, Hayashi discloses a method of fabricating an SOI structure comprising:

(a) providing a substrate 21 (Fig. 2B) having at least one of active or passive elements on a surface thereof (i.e. the "first layer device" 22);

(b) providing a device wafer 14, 15 having at least one of active or passive elements on a surface thereof (i.e. "second layer thin film device" 23);

(c) forming an electrically insulating layer 17 having opposed faces on the surface of one of the substrate and the device wafer and having an electrical interconnect structure 18 therewithin and extending to at least one face; and

(d) bonding said electrically insulating layer to the substrate at the bond region 13, a refractory metal bump, wherein the interconnect structure 18 contacts the bond region (Figs. 2B-2C).

Note that on page 7, lines 5-7 of Appellant's specification, layer 5 is referred to as the "device layer 5" which is shown only as a layer in Appellant's figures **without** any specific "passive" or "active" elements as claimed. Compare to either of 22 or 23 in Fig. 2B of Hayashi, as noted above, which shows the same nondescript "first layer device" or "second layer thin film device.")

Regarding claims 7-9, Hayashi discloses a method of fabricating an SOI structure comprising:

providing a substrate 21, 22 (Fig. 2B), with a planar surface, having at least one of active or passive elements on a surface thereof (i.e. the "first layer device" 22); a device wafer 14, 15, 23, with a planar surface, having at least one of active or passive elements on a surface thereof (i.e. "second layer thin film device" 23); and an electrically insulating layer 17 having an electrical

interconnect structure 18 therewithin and extending to a surface thereof, said interconnect structure separating a portion of said device layer from said substrate;

Regarding claims 18-21, and 23-24, Hayashi discloses a method of fabricating an integrated circuit comprising:

(a) providing a device layer 23 having devices (Fig. 2B);

(b) providing a substrate 21 having devices 22 thereon;

(c) providing a dielectric 17 bonded to one of said device layer and said substrate having an interconnect 18 disposed therein and extending to at least one surface thereof; and

(d) then bonding said dielectric to the other of said device layer and said substrate to form an interface with said one of said device layer and said substrate and forming an electrically conductive path across said interface to said interconnect.

See also columns 3-4 and column 5, lines 11-16.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 7-9 and 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi** in view of Appellant's admitted prior art (**APA**).

Hayashi, as indicated above, discloses all of the features of the instant invention except for applying a voltage across an electrically insulating layer to break down said portion of said electrically insulating layer.

On page 7, lines 7-12, **Appellant** indicates that it is known in the art to break down oxide by applying voltage across an electrically insulating layer by stating,

> "In the event a thin native oxide has developed over the device wafer 5 or the substrate 1 or the flowable dielectric insulates the interconnect in the electrically insulating layer from the substrate or device wafer, **a sufficiently high voltage can be passed through the circuitry involving the interconnect 7 to cause breakdown of the native oxide or the other dielectric** and allow completion of the connection **as is well known in the art.**" (Emphasis added; specification page 7, lines 7-12.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify **Hayashi** by Appellant's **APA** because native oxide (i.e. the electrically insulating layer) inherently forms on all metals (perhaps with the exception of gold) upon exposure to air -- and, in particular, would form on **Hayashi's** refractory metal bump and indium metal pool -- and Appellant admits that it is known in the art for such dielectric to form incidentally, and that it should be removed in order to establish the electrical connection, by the known art means of applying an electrical voltage.

(11) Response to Argument

Regarding **ISSUE 1**

Appellant states that "Claims 1 to 4, 7 to 9, and 18 to 24 were rejected under 35 U.S.C. 102(b) as being anticipated by Hayashi (U.S. 5,087,585)." This is an **inaccurate** statement of the claims rejected over Hayashi. Appellant's Representative, nonetheless, correctly stated the rejected claims under the applied statute under the section entitled, "ISSUES" at the beginning of the same page 3. Instead, claims 1, 3, 7-9, 18-21, 23, and 24 are rejected under 35 U.S.C. 102(b).

Appellant argues, "There is no build-up of layer upon layer as is found in Hayashi." This is an irrelevant argument because (1) no such limitation is claimed, (2) no such limitation is distinguished by the claim language, and (3) Appellant's invention builds up layer upon layer to the same extent that Hayashi does. Appellant's specification, page 8, lines 8-9, states, "One option is to form the dielectric 3 in layers with **multiple levels of interconnect** 11 as illustrated in FIGURE 3." (Emphasis added.) Appellant's specification, page 8, lines 8-9, states, "Various dielectric materials or composites thereof can be used to form layer 3, such as, for example, grown oxides, **deposited** oxides, and nitrides." (Emphasis added.) Appellant's claim 1 states, "forming an electrically insulating layer having a pair of opposed outer faces...**on said surface** of one of said substrate or said device wafer." (Emphasis added.) In each of the aforementioned instances, the invention a dielectric layer is formed upon another layer (device wafer or substrate) -- not to mention "multiple levels of

interconnect." This is clearly build up of layer upon layer and is also no different from what Hayashi does in Figs. 1D to 1E wherein a dielectric layer 17 is formed upon the device layer 16. Therefore, Appellant's argument is both moot and without merit.

Appellant argues, on page 3, last paragraph, "Furthermore, the interconnect is disposed within the dielectric layer. No such arrangement is found in Hayashi." Similarly, Appellant argues on page 4, first full paragraph, "There is no interconnect in Hayashi and, in the event the non-refractory metal pool 18 is alleged to be such interconnect, which it is not, this element is not disposed within the insulative layer 17." Examiner respectfully disagrees noting that Appellant's Representative's statements clearly contradict the teachings of the applied art. The refractory metal pool is, in fact, interconnect both by definition and by its explicit use in Hayashi. Hayashi, column 3, lines 49-53, states "A non-refractory metal is filled to the opening formed in the rear insulative layer 17 so as to form, as an undersurface connection electrode, a non-refractory metal pool 18..." Furthermore, and perhaps more importantly, Hayashi states in column 5, lines 11-15, "Furthermore, it would be apparent that the present invention can be applied to **stacking** of devices formed on semiconductor substrates other than a silicon substrate and **also of wiring layers formed on insulative substrates.**" (Emphasis added.) This statement clearly demonstrates that Hayashi also intends the use of his method for forming multiple levels of wiring layers (i.e. "multiple levels of interconnect" as coined by Appellant). Hayashi uses the non-refractory metal pool to form a single or multiple wiring layers for electrical connections between devices on different layers (device layers 22, 23).

The refractory metal pool 18 is therefore, by definition, interconnect, because it forms electrical connections between separate devices. It is also necessarily "disposed within the insulative layer" to every extent that Appellant has claimed. The non-refractory metal pool 18 is explicitly shown and stated to be within the dielectric layer 17. The explicit use and showing of interconnect 18 disposed within an insulative layer 17, clearly shows Appellant's argument to be without merit.

Beginning with the last sentence on page 3, Appellant further argues,

> "Still further, any insulation buildup between the interconnect and the device in the substrate to which interconnection is to be made is obviated by the application of a sufficiently high voltage across the insulation buildup, **when necessary**, between the interconnect and the device in the substrate to break down the intervening insulation and provide contact between the interconnect and the device in the substrate of device layer. It follows that the structures of Hayashi and the subject invention and the method of fabrication of the two are entirely different and unrelated to each other." (Emphasis added.)

The issue of the incidental build-up of dielectric material which impedes the electrical interconnect is **not** rejected under **Hayashi alone**. but is instead rejected under Hayashi in view of Appellant's admitted prior art, as noted above in the rejection. Since Appellant's Representative has ventured the argument presently and has not addressed it at all in its appropriate location under "ISSUE 2," it will be addressed here.

In as much as the build-up of dielectric is (1) incidental, (2) undesired, (3) is ultimately broken down to eliminate it, and (4) is admitted prior art, Appellant's use of this limitation to distinguish instant invention from Hayashi in view of Appellant's APA, is without merit. As repeated from the rejection above, on page 7, lines 7-12, **Appellant** indicates that it is known in

the art to break down incidental build-up of insulative material by applying voltage across the electrically insulating layer by stating,

> "In the event a thin native oxide has developed over the device wafer 5 or the substrate 1 or the flowable dielectric insulates the interconnect in the electrically insulating layer from the substrate or device wafer, **a sufficiently high voltage can be passed through the circuitry involving the interconnect 7 to cause breakdown of the native oxide or the other dielectric** and allow completion of the connection **as is well known in the art.**" (Emphasis added; specification page 7, lines 7-12.)

No further addressing of this argument is deemed necessary because the claims presently rejected under Hayashi alone do **not** have this limitation. Nonetheless, Appellant clearly provides the appropriate suggestion to use such a known method.

Regarding the remainder of page 4 of Appellant's arguments which are directed to claim 1. Appellant restates without argument that Hayashi lacks (1) the formation of the "electrically insulating layer with a pair of opposed outer faces...disposed on one of the substrate or the device wafer;" (2) the interconnect structure (18 in Hayashi) extending substantially to the one of the outer faces of the electrically insulating structure (17 in Hayashi) to make electrical contact with a device (either 22, or 23 in Hayashi) in at least one of the device wafer and the substrate, but each of these features is clearly shown in Hayashi as indicated in the rejections above.

Further in this regard, Appellant's Representative argues, "The pool of Hayashi is not disposed at a surface of the electrically insulating structure and is not shown as being connected to anything in the second layer thin film device 23 other than the layer itself." Examiner notes with interest that this is exactly how Appellant has portrayed his interconnect

(as noted in the rejection above), with the interconnect connected to nothing but the device layer itself. (See device layer 5 and interconnect 7 in Appellant's) Figures 1-3. It is therefore, wholly improper for Appellant's Representative to distinguish the present invention from Hayashi on the basis of the same thing that is absent in Appellant's invention. Nonetheless, interconnect is used for electrically connecting devices (hence the name); it is not randomly strewn on or in a semiconductor device without purpose. It's art known purpose renders the actual showing of the devices themselves unnecessary, as clearly intended by the equivalent absence in Appellant's own figures. Therefore, the argument forwarded by Appellant's Representative is without merit.

Beginning in the last sentence of page 4, Appellant's Representative argues that Hayashi teaches a different order of steps. Examiner is perplexed. Figures 1D to 1E show the formation of the insulative layer 17 with the interconnect 18 contacting the device layer 16 so this order of steps is taught. In Figures 2B to 2C, the substrate is next bonded to the device wafer. The Hayashi figures clearly show the same order of steps as claimed by Appellant. Examiner does not know what else to say.

On page 5, Appellant makes arguments regarding claims 2-4 and 7, but claims 2 and 4 are **not** rejected under Hayashi **alone**. Again Appellant's Representative is in error for suggesting otherwise. Nonetheless, the issues of claims 2 and 4 will be addressed here, in deference to Appellent's Representative, since they are not otherwise addressed under there proper location, "ISSUE 2." Claims 2-4 have been addressed above. They further limit claim

1 by admitted prior art limitations of breaking down an incidentally formed insulating layer, as noted above, and are not believed to require further mention except to say that the rejection of claims 2 and 4 is over Hayashi in view of Applicant's APA and is proper for the reasons indicated in the rejection.

Regarding claim 3, Appellant's representative alleges that Hayashi does not have a "bond region." Examiner respectfully disagrees. The bond region is the region where the interconnect either of the device layers or the refractory metal bump13. Examiner notes with interest again, that Appellant's figures also fail to show any explicit "bond region" in Appellant's Figures. As similarly noted above, Appellant's failure to show such bond regions makes such allegations of their absence in the applied art improper and without merit.

Regarding claim 7, the only additional feature not already claimed in claim 1 are that the surfaces have a "substantially planar region" on said device layer, and said substrate. The Hayashi Figures clearly require such "substantially planar regions" to enable bonding of the wafers. Again the argument is without merit, as the feature is present, but only alleged absent without a showing why the surfaces do not have a planar region.

Claims 8 and 9 are again alleged to be absent the clear and present interconnect 18 in the insulative layer 17. Again no argument, only allegation.

Claim 18, the **broadest** of the independent claims, clearly has each of the features of claims 1 and 7 and again no arguments are presented by Appellant's Representative to indicate

why the features clearly shown in the applied art are absent. Each of the features is, again, merely alleged absent.

Regarding claims 20 and 21, the electrically conductive path is clearly an extension of the device layer as shown, for instance as the refractory metal bump 13 in Figure 2B in Hayashi. Note claim 18, states, "(d) then bonding said dielectric to the other of said device layer and said substrate to form an interface with said one of said device layer and said substrate and forming an electrically conductive path across said interface to said interconnect" and claims 20 and 21 state, "wherein said electrically conductive path is an extension of said device layer." There exist no restrictions on the extension of the device layer. Therefore, the refractory metal bump is appropriately considered the extension because it extends from the device layer 22 and forms the electrical connection.

Claim 22 is, again, not rejected over Hayashi alone, but over Hayashi in view of Appellant's APA. It is the same subject matter of claims 2 and 4 and is rejected for the same reasons. No additional arguments have been presented by Appellant's Representative.

In arguing claim 23, Appellant's Representative apparently believes that the substrate 21 in Hayashi is not a "semiconductor" substrate, even though it is clearly labeled as "Si-substrate," wherein Si is the notoriously well known chemical symbol for silicon, the most widely used semiconductor substrate in the semiconductor fabrication industry.

In arguing claim 24, not only does Appellant's Representative apparently not believe that the substrate 21 in Hayashi is not a "semiconductor" substrate, but also that it does not

have a dielectric layer in spite of the fact that one is clearly deposited, specifically 17. Again there is no argument as to why the dielectric layer 17 in which the interconnect 18 is formed is somehow not a dielectric a part of the substrate.

In responding to previous of Examiner's response to arguments forwarded by Appellant's Representative, Appellant's Representative states, "the Examiner appears to have a misunderstanding as to what is being argued and what is his or her function." Examiner wholly disagrees. Examiner simply cannot respond to mere allegations of the absence of a clearly shown feature without some indication as to why such features are not those claimed in the invention at issue. This demotes the examination process to tag game of he-said-she-said with no means to resolve the differences. Hence arguments are **essential** when a discrepancy exists as to what a patent shows in order to establish differences between what an applied reference shows and what an application being examined shows. Appellant's Representative has failed and continues to fail to provide such arguments.

Finally, Appellant's Representative states,

> "With reference to the Examiner being perplexed as to the position of appellant as to the interconnect 18 of Hayashi, this is a metal pool and is not at the surface of the interconnect to which reference is being made. The metal pool 18 of Hayashi is disposed in an aperture in a layer 17 and is otherwise unrelated to the layer 17 in any way. This structure does not read on that which is being claimed."

Examiner remains perplexed. And again, there is no substantive argument presented. As stated above, the refractory metal pool 18 serves a specific purpose of electrical connection as expressly stated by Hayashi.

Regarding the "surface of the interconnect to which reference is being made," the claimed surfaces are that of the device layer and the substrate. No reference is made to any specific surface of the interconnect. Instead, the claims indicate that the interconnect contact one or the other of the device layer or the substrate which it must do to establish an electrical connection. The claims also state that the interconnect extends substantially to at least one of the surfaces of the dielectric layer which is clearly shown in both the Hayashi and Appellant's Figures. Examiner does not know what point is trying to be made.

Regarding the non-refractory metal pool 18 being "otherwise unrelated to the [insulative] layer 17 in any way, Examiner is especially perplexed. Appellant has not claimed or disclosed any "relationship" between them, other than that the interconnect is disposed in the insulative (dielectric) layer 17 as shown in both Hayashi and in Appellant's Figures. And as noted above, Hayashi states that his invention is for use with multiple interconnect ("wiring" layers), so again there is no difference between the interconnect shown in Appellant's Fig. 3 and that disclosed, but not shown, in Hayashi.

Taken as a whole or individually, Examiner respectfully asserts that Appellant's arguments are without merit. According to Appellant's Representative, not a single feature of the instant

invention is in Hayashi or in Hayashi in view of Applicant's APA, not even the feature that the substrate is a semiconductor material even though Hayashi shows that it is made of the most well known semiconductor, silicon. When features which are most clearly present in Hayashi are merely alleged to be absent by Appellant's Representative without any supporting argument as to why the noted features of the applied art are not those presently claimed, it is not possible for Examiner to address the allegations beyond referring the Board to the rejections above.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

EK
August 13, 2001

An appeal conference was held on 8/13/01 with, in addition to the above signatory, the following attendees:

Arthur T. Grimley, SPE of Art Unit 2852 _____

Charles L. Bowers, Jr., SPE of Art Unit 2813 _____

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